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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,983	07/21/2003	Zhijian Xie	3-4	5529

7590 05/04/2005

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EXAMINER	
ABRAHAM, FETSUM	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,983	XIE ET AL.	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "112" and "124" have both been used to designate the same "oxide" layer on the substrate in figure 1. "112" should be extended down to point at the gate electrode beneath the insulation layer as taught in page 4, lines 5 and 21 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "DUMMY GATE" has been used to designate both said dummy gate and said and shielding electrode (222) in figure 2. The upper dummy gate pointer must be deleted. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top

margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the shielding layer position in claim 1 in relation to the claimed vertical DMOSFET and specifically its connection to said first/source region through said vertical conductor and its positional relation ship with said gate and second source/drain region in view of the 90 degrees physical change of the device in claim 1.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.**

Claim 1,2,5-8,11-16,18 are rejected under 35 U.S.C. 102(a) as being anticipated by Morikawa et al (6,707,102).

As for claims 1,2,7,8,11,12,14,16 the prior art structure in the front page discloses a power LDMOSFET composed of a substrate (1) of the first conductivity

type, first source/drain region of the second conductivity type (5) in the substrate, a second source/drain region (9) formed in the substrate and spaced apart from the first source/drain region, a gate (3) proximate the upper surface of the semiconductor layer, a shielding layer conductor (10) analogous to the claimed shielding layer formed proximate the upper surface of the semiconductor layer and between the gate (3) and the second source/drain region (9), the structure being electrically connected to the first source/drain region by way of a connection comprising a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate (3) and the second source/drain region (9) and the shielding layer laterally spaced from the gate and not overlapping with the gate.

As for claims 2,5,15 a conductive trace spaced substantially from the gate by an oxide insulation layer on the substrate connects the shielding layer (10) to the first source/drain region (the source region from now on).

As for claim 6, layer (5) and layer (9) of the prior art are source and drain regions of the structure.

As for claims 11,13, the abstract teaches that the shield conductive layer was electrically connected through via in an insulation film and stays parallel with the drain electrode structure, which is connected to the drain region through conductive plugs penetrating the insulation layers (12,22). The shield layer wiring, no matter how small it looks in the drawings passes through the same insulation layers to qualify for a plug.

As for claim 12,18 the gate is a multilayered structure composed of at least two layers that guarantee minimized gate resistance.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 3,4,10,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa et al.

Although the prior art may be silent on the claimed method of forming said conductive trace, the claimed method has no patentable substance in view of the device claimed in claim 1 so long as the end product converges to the same structure.

Claims 3 and 4 are related as process of making and process of using the product. The use as claimed cannot be practiced with a materially different product. Since the product is not allowable, restriction is proper between said method of making and method of using. The product claim will be examined along with the elected invention (MPEP § 806.05(i)).

As for the functional language of claims 10,17, capacitance between the gate and the shielding structure (10) of the prior art is minimized (see column2, 45-60) and figure 19. Although the prior art may be silent about the gate/source capacitance behavior in view of the existence of said shielding layer, it would have been obvious to one skilled in the art to safely assume that the shielding layer has no impact in that capacitance due to the constant positional with the source region in relation to the gate electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
4/28/05